Voltage Control System for LC-RIS

A Scalable, Low-Latency Hardware-Software Control System for Liquid-Crystal Based Reconfigurable Intelligent Surfaces

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Abstract

Liquid-crystal reconfigurable intelligent surfaces promise agile 6G links, yet they need hundreds of independent, stable bias voltages; existing drivers are slow, pricey or hard to scale. We built a low-cost, scalable 64-channel controller that synthesises one 1 kHz ±10 V square-wave reference and tailors its amplitude per element through an 8-bit digital potentiometer-op-amp chain. A Raspberry Pi Pico updates all 64 amplitudes in 124 μs, comfortably inside the millisecond response window of liquid crystals. Tests confirm accurate waveform generation across all channels, showing the concept's feasibility and affordability. The architecture can extend to larger panels, though long-term large-scale stability remains a task for future validation research.

1 Background

Reconfigurable Intelligent Surfaces (RIS) are two-dimensional arrays of programmable elements that shape the radio environment for next-generation 6G networks. LC-RIS is a type of RIS that uses liquid crystal materials.

2 Research Question

Main

What is a scalable, low-latency hardware-software solution for controlling LC-RIS systems?

- **Hardware**: drive ≥ 50 channels, ±10 V min., ≥ 7-bit resolution
- **Waveforms**: synchronized 1 kHz square waves
- **Latency**: API-to-voltage update < 1 ms
- **Scalability**: maintain specs as channel count grows
- **Validation**: well-defined tests and metrics

3 System Architecture

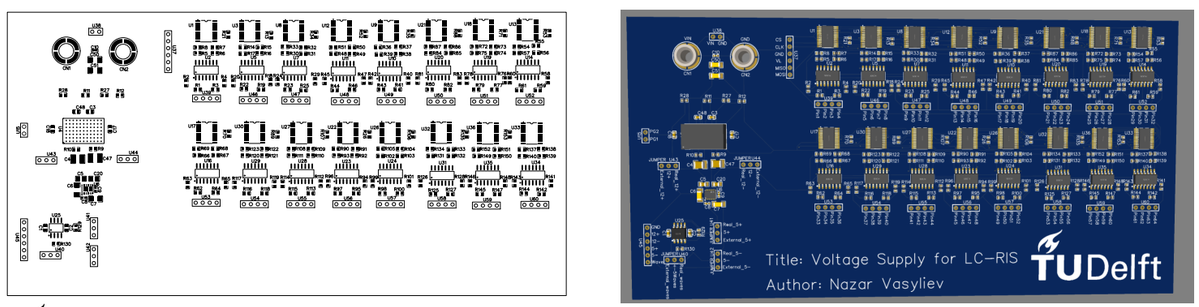
The system combines a centralised analog waveform generator with distributed digital amplitude control.

The master oscillator is built around a classic NE555 timer IC to output a ∼1 kHz square wave. This simple analog oscillator produces a base AC signal that is shared by all channels, guaranteeing that every LC element sees a synchronised, in-phase drive without per-channel timing drift. We power the NE555 from ±5V rails so it's forming an approximately ±5V reference square wave.

Per-Channel Amplitude Control: To provide each LC cell with an independent bias voltage, the 64 channels each use an AD5263 digital potentiometer (8-bit resolution) in series with a high-input impedance op-amp OPA4197 configured as a buffer/amplifier (with gain of 2). The digital potentiometer acts as a programmable voltage divider that scales the ±5V reference to the required amplitude, and then OPA4197 drives it up to ±10 V for that channel.

Microcontroller and Communication: A Raspberry Pi Pico microcontroller running MicroPython handles the system's logic. The Pico communicates with the 16 AD5263 potentiometer chips (each IC carries 4 channels) over a daisy-chained SPI bus. By sending one 160-bit frame, the Pico updates all 16 channel values simultaneously. Settings new values to all channels (4 data frames, 16 channels each) takes only ∼124 μs. The SPI chain is easily extendable, meaning more channels can be added.

Power Supply: The module uses LTM8049 to generate stable ±12 V rails from an input source. These ±12 V rails feed the op-amps (for full ±10 V output swing headroom) and also pass through a LT3032-5 to produce the ±5 V rails used by the NE555 and digital potentiometers.



(a) PCB schematic

(b) 3-D rendered PCB

Figure: Simulation result and corresponding board layout

4 Results

Table: Power-rail voltages under various operating conditions

Condition	V_{-5} (V)	V_{+5} (V)	V_{-12} (V)	V_{+12} (V)
Expected	-5.00	+5.00	-12.00	+12.00
No load (cold)	-5.02	+5.04	-12.10	+12.10
Full load, cold	-5.04	+5.06	-12.10	+12.10
Full load, hot	-5.02	+4.15	-12.20	+12.10
Full load, external +5, cold	-4.99	+4.94	-12.10	+12.10
Full load, external +5, hot	-5.00	+4.94	-12.10	+12.10

Waveform Generation (Frequency and Duty Cycle): The NE555 master clock was intended to output a 1.0 kHz, 50% duty cycle square wave, but the measured frequency came out consistently around 820-833 Hz with a ∼ 58% high duty cycle. This 17% lower frequency is explained by RC tolerances in the NE555's timing network, and power rails are not perfectly equal by modulus.

In practice, the actual resistor and capacitor values deviate from their nominal specifications (often by ±10%), which directly skews the oscillation frequency and duty cycle. Despite this discrepancy, the output remained a clean, stable square wave, and the ∼0.83 kHz rate still meets the system requirements (the LC cells tolerate a broad range around 1 kHz). In future iterations, if higher precision is needed, we could improve the oscillator by using tighter-tolerance components or replacing the NE555 with a more precise timing source (e.g. a CMOS 555 variant or a microcontroller-based oscillator).

Power Rail Performance: During testing, we observed that the +5 V supply rail was not stable under full load. In a worst-case scenario (all 64 channels at maximum output, after the system had warmed up), the nominal +5.0 V rail dropped to about +4.15 V. This sag was traced to the on-board linear regulator's current limit. The LT3032-5 regulator sourcing +5 V is rated for 150 mA; at full load the NE555 oscillator and digital potentiometers together drew a current exceeding this limit as temperature increased. Hitting the current limit caused the regulator output to droop below 5 V. This explained why the waveform's positive peak dropped in the "hot, full load" condition (Table 1). Notably, the ±12V rails remained rock-solid around ±12.1V throughout, since the LTM8049 can supply enough current for the op-amps without issue. To resolve the +5 V sag, we temporarily powered the +5 V rail from an external bench supply for testing. With a sufficiently capable external 5 V source, the rail held at ∼4.94 V under the same full-load, hot conditions. For a permanent fix, the power regulator could be upgraded: e.g. use a higher-current LDO or a switching regulator for the +5 V rail.

Multi-Channel Output Accuracy: Aside from the two issues above, all other performance metrics met the design goals. Each of the 64 channels successfully produced a ±10 V peak-to-peak square wave with the commanded amplitude setting. At the maximum setting (255), channels reached roughly ±10.4 V, which is very close to the intended ±10 V output. This slight overshoot is due to the op-amp headroom and tolerances.

Update latency was empirically confirmed, as issuing a batch update from the Pico resulted in all channels settling to new voltages in tens of microseconds, under the 1 ms requirement (in line with the ∼124 μs SPI transfer time). This means the system can effectively "stream" new configurations to the LC-RIS in real time without lag.

5 Conclusion

We demonstrated a 64-channel LC-RIS driver that pairs a simple NE555 clock with digipot-trimmed voltages, proving an analog-distribution/digital-control architecture that can scale to hundreds of channels. Tests revealed two straightforward fixes, guiding the next design spin: compensating timer drift and giving more current headroom to the 5 V rail. With those upgrades and long-term LC-panel trials, the platform can power large, fast-tunable metasurfaces for future 6G systems.

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